CLAIMS

What is claimed is:

1. A method of varying transconductance of a transconductance cell, wherein the cell comprises a first and a second load element, a first transistor coupled to the first load element, a second transistor coupled to the second load element, and a current source coupled to both the first and second transistors, the method comprising:

varying the size of the first and second transistors; and

varying a bias current from the current source.

2. The method of Claim 1, wherein the size is the aspect ratio (W/L).

3. The method of Claim 1, further comprising varying the impedance or resistance of the first and second load elements.

4. The method of Claim 1, wherein varying the size and varying the bias current are performed together.

5. The method of Claim 1, wherein varying the size and varying the bias current maintains a fixed ratio to maintain linearity.

6. The method of Claim 5, wherein the fixed ratio is a gate overdrive voltage given by $\sqrt{\frac{2I_D}{\beta \frac{W}{L}}}$, where where I_D is the drain current, W is the transistor widths, L is the transistor lengths, and β is equal to μC_{ox}, where μ is

the mobility, and C_{ox} is the capacitance associated with the gate oxide of the transistors.

7. The method of Claim 1, wherein the size and the bias current are varied digitally.

8. The method of Claim 1, wherein the first and second transistors are MOS transistors.

9. A programmable transconductance cell, comprising:

a voltage source;

a differential transistor pair comprising a variable sized first transistor and a variable sized second transistor;

a first load element coupled between the voltage source and the first transistor;

a second load element coupled between the voltage source and the second transistor; and

a variable current source coupled to the source of the first and second transistors.

10. The transconductance cell of Claim 9, wherein the first and second transistors are MOS transistors.

11. The transconductance cell of Claim 9, wherein the first and second load elements are passive load elements.

12. The transconductance cell of Claim 9, wherein the first and second load elements are active load elements.

13. The transconductance cell of Claim 9, where the variable current source is a digitally controlled variable current source.

14. The transconductance cell of Claim 9, wherein the first and second transistors are digitally controlled variable sized transistors.

15. The transconductance cell of Claim 9, wherein the first and second transistors are sized by adjusting the aspect ratio of the transistors.

16. An N-stage transconductance circuit, comprising:

a voltage source;

a first programmable transconductance cell coupled to the voltage source, the cell comprising:

a first differential transistor pair comprising a variable sized first transistor and a variable sized second transistor, wherein the gate of the first and second transistor are configured to receive differential input signals;

a first load element coupled between the voltage source and the first transistor;

a second load element coupled between the voltage source and the second transistor; and

a first variable current source coupled to the source of the first and second transistors, wherein a first differential output signal of the circuit is received from the drain of the first and second transistors; and

a control circuit for varying a current in the current source and the size of the first and second transistors.

17. The circuit of Claim 16, wherein each stage uses the same first variable current source and same differential input signals.

18. The circuit of Claim 16, further comprising a second variable current source, wherein a first stage uses the first variable current source and a second stage uses the second variable current source.

19. The circuit of Claim 18, wherein each stage uses the same differential input signals.

20. The circuit of Claim 16, wherein each stage uses different differential input signals.

21. The circuit of Claim 20, wherein each stage uses the same first variable current source.

22. The circuit of Claim 20, further comprising a second variable current source, wherein a first stage uses the first variable current source and a second stage uses the second variable current source.

23. The circuit of Claim 16, further comprising a second differential transistor pair, wherein each stage uses the same differential input signals.

24. The circuit of Claim 23, wherein a first stage output is the first differential output signal and a

second stage output signal is received from the drains of the second differential transistor pair.

25. The circuit of Claim 16, wherein N is the number of gain stages.

26. The circuit of Claim 16, wherein fingers in the current source and differential pair for each of the N stages are binary weighted.

27. The circuit of Claim 26, wherein N is at least two, with fingers in the first stage weighted by one and fingers in the second stage weighted by two.

28. The circuit of Claim 26, wherein each stage k of the N stages is weighted by 2^k, where k = 0 to N-1.